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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	6

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,278	KOZLOWSKI ET AL.	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 24-28* is/are allowed.

6)☒ Claim(s) *1-3,11,20 and 23* is/are rejected.

7)☒ Claim(s) *4-10,12-18,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "Q24" has been used to designate both source follower and access transistor. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim1 is rejected under 35 U.S.C. 102(e) as being anticipated by Levy (US Patent # 6, 147,340).

[Claim 1]

Levy teaches the following:

A photodetector amplifier circuit comprising:

a photodetector (figure 1: 10);

an input transistor connected to the photodetector (figure 1: 12);

an integration capacitor connected to an output of the input transistor (figure 1: Csubint);

and

an adaptive skimming circuit connected to the integration capacitor (figure 1: Q1 and 22, col. 5 lines 7-16)[The skimming circuit is adaptive in the sense that if a system having a variable integration time is used the number of times and when a skimming pulse is to be generated during the integration period can be changed as part of the overall system design (col. 6 lines 55-57). For example, as disclosed in figure 2b the skimming pulse is generated two times during an integration period, each of which removes a same quantity of charge Qsk (col. 6 lines 44-54)].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US Patent # 6, 147,340) in view of Wynen et al. (US Patent # 6,578,154).

[Claim 2]

Levy teaches an adaptive skimming circuit which comprises:

current source transistor (figure 1: Q1, col. 5 lines 7-10). Levy fails to teach a programming capacitor connected to the current source transistor and a programming transistor connected to the current source transistor and the programming capacitor. However these limitations are well known in the art as evidenced in Wynen (col. 5 lines 31-37)[Figure 7 discloses a current source 400 in which capacitor 404 and transistor 402 can be programmed independently as current references to program other NFET and PFET current sources). Therefore taking the combined

teachings of Levy and Wynen it would have been obvious to one skilled in the art to have the pulse generator (Levy, figure 1: 22) of Levy incorporate a programming capacitor (Wynen, figure 7: 404) connected to the current source transistor (Levy, figure 1: Q1) and a programming transistor (Wynen, figure 7: 402) connected to the current source transistor and the programming capacitor. Doing so (Programming the capacitor and transistor) would allow the relative sizes, process variables, and environmental conditions (e.g. temperature) of the circuits to be taken into account as taught in Wynen (col. 5 lines 17-20).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US Patent # 6, 147,340) in view of Wynen et al. (US Patent # 6,578,154) in further view of Ivanov (US Patent # 6,150,883).

[Claim 3]

Levy teaches an adaptive skimming circuit wherein a reset transistor (figure 1: 20. It is obvious to one skilled in the art that a reset switch can be implemented with a transistor) is connected to the input transistor (figure 1: 12) but Levy and Wynen fail to teach a cascode transistor connected to the current source transistor and the input transistor. However these limitations are well known in the art as evidenced in Ivanov [col. 2 lines 22-28, figure 2: 25 (cascode transistor) the first electrode is connected to 23 (current source) and the second electrode is connected to 13 (input transistor)]. Connecting of cascode transistors to current sources in a circuit enhances the operating speed of the circuit as disclosed in Ivanov (col. 1, lines 54-59, col. 2 lines 22-28). Therefore taking the combined teachings of Levy, Wynen and Ivanov it would have been obvious to one skilled in the art to have an adaptive skimming circuit of Levy to incorporate a cascode transistor connected to the current source transistor and the input transistor. Doing so

would make the circuit faster and operable at lower voltages resulting in higher gain-speed-power figure of merit as evidenced in Ivanov (col. 1 lines 54-59).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US Patent # 6, 147,340) in view of Ivanov (US Patent # 6,150,883) in further view of Wynen et al. (US Patent # 6,578,154)

[Claim 11]

Levy teaches the following:

A pixel cell comprising:

an input transistor (figure 1: 12);

a photodetector coupled to the source of the input transistor (figure 1: 10);

an integration capacitor (figure 1: Csubint) for storing a charge proportional to an amount of incident light on the photodetector (col. 4 lines 1-9); and

an adaptive skimming circuit comprising:

a current source transistor (figure 1: Q1) connected across the integration capacitor ((figure 1: Csubint);

a reset transistor connected to the input transistor (Figure 1: 20)[It is obvious to one skilled in the art that a transistor is notoriously used in the art as a switch];

wherein a current source provided by the current source transistor (figure 1: Q1) sinks a set level of current during integration of a charge on the integration capacitor (col. 3 lines 1-5) [Skimming a fixed amount of charge from the capacitor means skimming a set level of current generated by the photodetector].

Levy fails to teach a cascode transistor connected to the current source transistor and the input transistor. However these limitations are well known in the art as evidenced in Ivanov [col. 2 lines 22-28, figure 2: 25 (cascode transistor) the first electrode is connected to 23 (current source) and the second electrode is connected to 13 (input transistor)]. Therefore taking the combined teachings of Levy and Ivanov it would have been obvious to one skilled in the art to have an adaptive skimming circuit of Levy to incorporate a cascode transistor connected to the current source transistor and the input transistor. Doing so would make the circuit faster and operable at lower voltages resulting in higher gain-speed-power figure of merit as evidenced in Ivanov (col. 1 lines 54-59).

Levy and Ivanov fail to teach a programming capacitor connected to the current source transistor and a programming transistor connected to the current source transistor. However these limitations are well known in the art as evidenced in Wynen (col. 5 lines 31-37)[Figure 7 discloses a current source 400 in which capacitor 404 and transistor 402 can be programmed independently as current references to program other NFET and PFET current sources). Therefore taking the combined teachings of Levy, Ivanov and Wynen it would have been obvious to one skilled in the art to have the pulse generator (Levy, figure 1: 22) of Levy incorporate a programming capacitor (Wynen, figure 7: 404) connected to the current source transistor (Levy, figure 1: Q1) and a programming transistor (Wynen, figure 7: 402) connected to the current source transistor and the programming capacitor. Doing so (Programming the capacitor and transistor) would allow the relative sizes, process variables, and environmental conditions (e.g. temperature) of the circuits to be taken into account as taught in Wynen (col. 5 lines 17-20).

7. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Levy (US Patent # 6, 147,340).

Levy teaches the following:

A method for skimming current in an amplifier circuit, the method comprising:

generating a signal proportional to an amount of light incident on a photodetector (col. 3 lines 49-51);

producing a sink current (col. 3 lines 1-5) [Skimming a fixed amount of charge from the capacitor means skimming the sink current generated by the photodetector]; and

reading out a signal that is proportional to the difference between the generated signal and the sink current (col. 3 lines 1-6)[Reading out the charge at the end of integration period after skimming a fixed amount of charge means reading a signal proportional to the difference between the generated signal and the skimmed charge].

8. Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Levy (US Patent # 6, 147,340).

[Claim 23]

An amplifier circuit for coupling infrared (IR) detectors (col. 1 line 45) to multiplexing readouts, the circuit comprising:

detector means for converting incident light to an input electric signal (figure 1: 10);

signal input means for transferring the input electric signal from the detector means (figure 1: 12);

storage means for storing a charge from the detector (figure 1: 12); and

skimming means for skimming off a predetermined level of the input electrical signal (figure 1: Q1 and 22, col. 5 lines 7-16)[Removing a controlled amount of charge means a predetermined level of the input electrical signal];

wherein the skimming means produces a sink current to skim off a signal read out from the storage means (col. 2 lines 48-54, col. 5 lines 7-16).

Allowable Subject Matter

9. Claims 4-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

a) As for claim 4, the prior art of record does not teach or fairly suggests an adaptive skimming circuit comprising a kTC-noise reducing capacitor connected between the programming transistor and the programming capacitor.

b) Claims 5-10 depend upon claim 4.

11. Claims 12-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

a) As for claim 12, the prior art of record does not teach or fairly suggests an adaptive skimming circuit comprising a trim capacitor.

b) Claims 13-18 depend upon claim 12.

12. Claims 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

a) As for claim 21, the prior art of record does not teach or fairly suggests producing a sink current by applying a trimming voltage to a trim capacitor.

b) Claim 22 depends upon claim 21.

13. Claim 19 is allowed.

a) As for claim 19, the prior art of record does not teach or fairly suggests an adaptive skimming circuit comprising a kTC-noise reducing capacitor connected between the programming transistor and the programming capacitor.

14. Claims 24-28 are allowed.

a) As for claim 24, the prior art of record does not teach or fairly suggests an amplifying circuit for coupling IR detectors to multiplexing readouts comprising a trim capacitor connected between the source of the programming capacitor and the gate of the current source transistor and a kTC-noise reducing capacitor connected between the source of the programming transistor and the gate of the current source transistor.

b) Claims 25-28 depend upon claim 24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5: 30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's primary examiner, Vu Le can be reached (703) 308-6613. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

YKA
January 23, 2004

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